

APPLICATION No.
09/879,197

APPLICANT
Michio KOMODA et al.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
2	"Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation", Proc. IEEE International Conference on Computer Aided Design, 1989, Peter R. O'BRIEN et al., IEEE		
2	"A Gate-Delay Model for High-Speed CMOS Circuits", Proc. 31 st ACM/IEEE Design Automation Conference, 1994, Florentin DARTU et al., The University of Texas at Austin, Austin, Texas 78712		
3	U.S. Application No. 09/878,352, Michio KOMODA et al., " Method of Producing Load for Delay Time Calculation and Recording Medium", June 12, 2001		
Examiner Signature	Date Considered		

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. SEND TO: Assistant Commissioner for Patents, Washington, D.C. 20231.

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